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Acquisition Board Design Based on Arm and FPGA for Image Data

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Abstract: In this paper, the new data acquisition system integrates signal conditioning, a data acquiring, data collecting and processing function into the single board based embedded system. The motive of this work is to obtain a high integration level architecture that allows signals to be conditioned, simultaneously acquired according to the external clock and triggers processed and transferred to data servers in real-time. In this task, a system of high-speed image data acquisition based on ARM and FPGA is designed according to the needs of actual system in image processing and image data transmission, which take full advantage of the flexibility of ARM and the parallel of FPGA. The choice of ARM architecture is a 32-bit embedded RISC microprocessor architecture, which has a rich instruction set and programming flexibility. FPGA has a great advantage in the speed and parallel computing, suitable for real-time requirements of image processing. And the design of the image data between the acquisition board and PC in real time remote transmission is completed using the Gigabit Ethernet interface.

Keywords: FPGA, ARM, Ethernet, camera.

I. INTRODUCTION

The first stage of any vision system is the image acquisition stage. After the image has been obtained, various methods of processing can be applied to the image to perform many different vision tasks required today. However, if the image has not been acquired satisfactorily then the intended tasks may not be achievable, even with the aid of some form of image enhancement. With the rapid development of imaging technology, image acquisition and processing systems in improving the automation of industrial production is more and more widely.ARM FPGA-based high-speed synchronous data acquisition program application background is well known that most of the exploration, observations were carried out in the harsh environment, and the accuracy of data, real-time all have higher requirements, and most of the cases Multi-parameter simultaneous measurement requirements.
The disadvantage of the current data acquisition systems consist of many devices which are connected through various cables to provide the requested functionality. A study has been launched to identify the limitation of the present acquisition system. During the study, a new data acquisition system based on Field programmable gate array (FPGA) and Advanced RISC Machines (ARM) technologies has been developed in order to realise the continuous data acquisition and real-time data transmission.

II. HARDWARE DESIGN

A. System Design

The FPGA is used for the control of image sensor, image data cache and peripheral chip timing generation. FPGA realizes data acquisition by controlling the A/D and save to the SRAM, decodes the read and write signals of the ARM into read back the target data and spread to the PC.

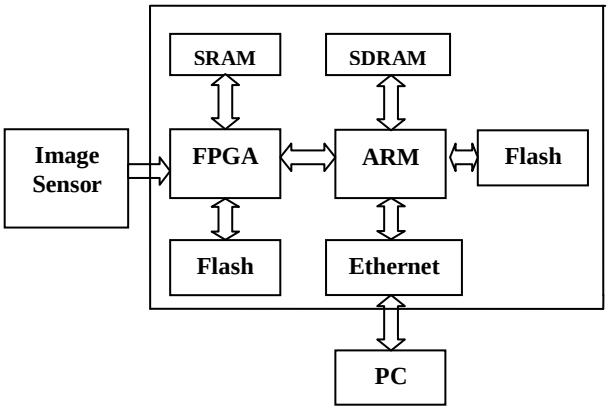

Fig. 1: Block diagram of image data acquisition board

The ARM is responsible for the overall control of the system, which completes instructions and data transmission by the address of read and write bus. ARM connected with the Ethernet controller by bus is the subject of communication control. ARM realizes Ethernet controller internal registers programming through the network driver, as well as sending and receiving Ethernet data, thus completing the network and data transfer between systems.
The flash chips can store different FPGA configuration files each implementing different signal processing algorithms or different parameter. A remote user, via the microcontroller Ethernet interface, can select from these configuration files and load it into the FPGA.

B. Image Acquisition

For capturing an image uCAM-II (microCAM-II) is used. The uCAM-II (microCAM-II) is a highly integrated serial camera module which can be attached to any host system

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that requires a video camera or a JPEG compressed still camera for embedded imaging applications.

The module uses a CMOS VGA colour sensor along with a JPEG compression chip that provides a low cost and low powered camera system. The module has an on-board serial interface (TTL) that is suitable for a direct connection to any host microcontroller UART or a PC system COM port. The uCAM-II is capable of outputting both RAW format and JPEG format images. User commands are sent using a simple serial protocol that can instruct the camera to send low resolution (80x60 to 160x120) single frame raw images for viewing or high resolution (160x128 to 640x480) JPEG images for storage or viewing.

The uCAM-II has a dedicated hardware UART that can communicate with a host via this serial port. When an INITIAL, GET PICTURE, SNAPSHOT, SET PACKAGE SIZE, or RESET command is sent to the camera, the camera will simply reply with an ACK if successful.

LPC1768-Xplorer

LPC1768-Xplorer is a breakout board for the NXP LPC1768 ARM Cortex-M3 microcontroller. The LPC1768 operates at up to 100 MHz. Its features include 512KB of internal Flash, 64KB RAM, Ethernet MAC, USB Device/Host/OTG interface, 8-channel general-purpose DMA controller, four UARTs, two CAN channels, two SSP controllers, SPI interface, three I2C-bus interfaces, 2-input plus 2-output I2S bus interface, 8-channel 12-bit ADC, 10-bit DAC, motor control PWM, Quadrature Encoder interface, four general-purpose timers, 6-output general-purpose PWM, ultra-low-power Real-Time Clock (RTC) with separate battery supply, and up to 70 general-purpose I/O pins.

Embedded system is a kind of special computer system which has limited resources and functions. To implement Web server in embedded system is characteristic of itself. The supported TCP/IP protocol is used. Considering the need of data exchange during equipment controlling is implemented through HTML.

The communication module is the interface between central processing unit and transceiver module. Its work is to receive data form transceiver and then transmit them to the ARM processor. Processor module is the core part of the design, in which the ARM chip LPC1768 is used to complete the complex operations and receive a lot of data from transceiver as a slave. In the module, data link between SPI port and Ethernet is established, SPI data stream format is specified, the transmission rate between serial data stream and IP data packets is controlled and IP packet is received or sent through reading or writing Ethernet interface module In the Ethernet interface module, the collected data are uploaded to a PC via Ethernet interface by using the functions of operating system and the commands from the host computer are received commands to control the data acquisition system.

Embedded C language has been used for the software implementation of the embedded web server. The web pages which are required for the web server were developed using HTML. This embedded web server is tested for its working, using a data acquisition web application hosted over a network of PC's.

The Ethernet block contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (**Media Access Controller**) designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with Scatter-Gather DMA off-loads many operations from the CPU.

The Ethernet block is an AHB master that drives the AHB bus matrix. Through the matrix, it has access to all on-chip RAM memories. A recommended use of RAM by the Ethernet is to use one of the RAM blocks exclusively for Ethernet traffic. That RAM would then be accessed only by the Ethernet and the CPU, and possibly the GPDMA, giving maximum bandwidth to the Ethernet function.

The Ethernet block interfaces between an off-chip Ethernet PHY using the RMII (Reduced Media Independent Interface) protocol and the on-chip MIIM (Media Independent Interface Management) serial bus, also referred to as MDIO (Management Data Input/output).

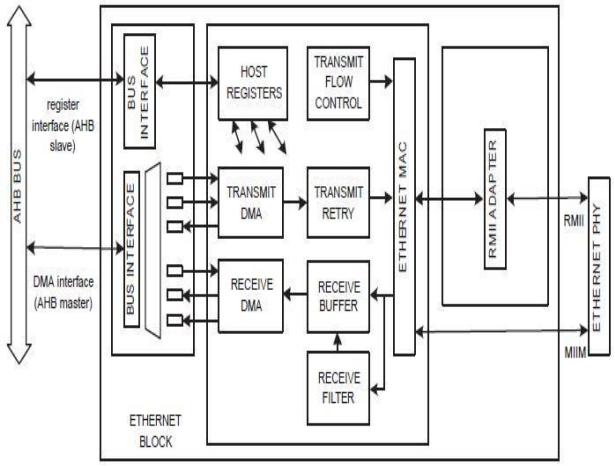

FIG.2: BLOCK DIAGRAM OF THE ETHERNET BLOCK OF LPC17XX

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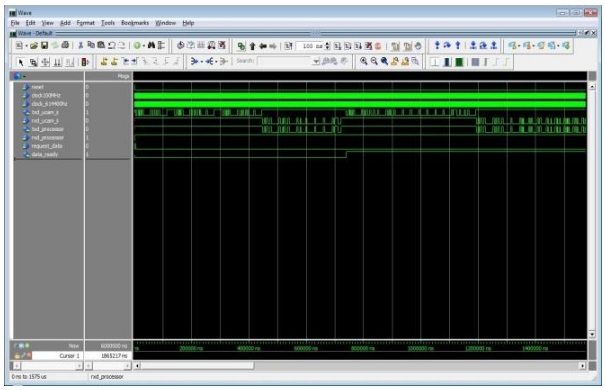
III. RESULTS



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